

STRUCTURAL INPUT LEVELS TESTING USING ON-DIE LEVELS GENERATORS

ABSTRACT OF THE DISCLOSURE

A set of levels generating circuits, such as a set of digital-to-analog converters, is designed into an integrated circuit on-die. The levels generating circuits apply direct current (DC) voltage levels to on-die sense amplifiers to test sense amplifier trip points for "input low voltage" (VIL) and "input high voltage" (VIH). The levels generating circuits are controlled by a set of configuration bits, which may be accessible through the boundary-scan register or the input/output (I/O) loop back pattern generator. The levels generating circuitry allows testing of one number of integrated circuit input pins using a smaller number of input pins.

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